DSG-SoLID R&D Meeting Minutes

Date: February 18, 2022
Time: 11:00 – 12:00

Attendees: *Mary Ann Antonioli, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran*

1. Cable fabrication and labeling

Pablo Campero and Mindy Leffel

1. Crimped terminal lugs to wires to ground the signal conditioning backplanes to the rack
2. Completed 19 of 64, 100' cables
3. Applied 24 and 5 VDC labels

2. Instrumentation rack debugging

Pablo Campero, Mindy Leffel, and Marc McMullen

1. Solved valve control issues
2. Debugging of voltmeter to monitor valve position of LVDT module in local mode is in progress
3. Tested constant current source boards
    - All six boards in rack worked as expected
    - Recorded voltage and current measurements of all boards